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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/650,800 | 08/30/2000 | Paul S. Neuman | RA 5290(33012/289/101) | 1186 |

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| EXAMINER |
|---|
| VITAL, PIERRE M |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 06/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/650,800 | NEUMAN, PAUL S. | |
| | Examiner | Art Unit | |
| | Pierre M. Vital | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is in response to applicant's communication filed June 12, 2003 in response to PTO Office Action mailed April 9, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-20 have been presented for examination in this application. In response to the last Office Action, no claims have been amended. No claims have been canceled or added. As a result, claims 1-20 are now pending in this application.

3. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Lynch et al. (US6,061,766).

As per claim 1, Lynch discloses a data processing system having a system bus {*i.e., common memory bus*} and having a processor with a level one cache memory {*i.e., CPU 302, on-board caches 308*} responsively coupled to a level two cache memory {*i.e., cache 306*} which is responsively coupled to a level three cache memory {*i.e., main memory*} [Fig. 3; col. 3, lines 36-43]; and having a circuit for Snooping said system bus [col.3, line 60]; and first logic which invalidates a corresponding level one cache memory location {*i.e., processor invalidate data in their own memories (or on-chip caches)*} in response to either a non-local write or write ownership request {*i.e., request for exclusive use*} [col. 1, lines 40-48, 53-55].

As per claim 2, Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership {*i.e., only requests for exclusive use which match cache tags are invalidated*} [Fig. 4; col. 4, lines 19-30].

As per claim 3, Lynch discloses third logic which invalidates said corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26].

6. Claims 6, 11 and 16 is rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. (US6,397,300).

As per claim 6, Arimilli discloses a data processing system comprising a level one cache memory {*i.e., CPU 150, L1 cache 200*}; a level two cache memory responsively coupled to said level one cache memory {*i.e., L2 cache 202*}; a system bus

[system bus 105; Fig. 4]; a level three memory responsively coupled to said level two cache memory {*i.e., main memory coupled to L2 cache 202*} [Fig. 4, col. 8, lines 30–49]; and a first circuit to invalidate a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory write {*i.e., if hit in upper level cache, cache line in upper level cache invalidated*} [col. 5, lines 12-25].

As per claims 11 and 16, Arimilli discloses a method of maintaining validity of data within a level one cache memory of a processor responsively coupled to a level two cache memory which is responsively coupled to a system memory bus [Fig. 4, *L1 cache 200, L2 cache 202, system bus 105*] comprising: formulating a write request {*i.e., issuing store operation*} [col. 12, lines 10]; first experiencing a level one cache memory miss in response to said write memory request [col. 12, line 18]; second experiencing a level two cache memory hit in response to said first experiencing step [col. 9, lines 33-34, col. 12, lines 54-56]; and invalidating a portion of said level one cache memory corresponding to said write memory request in response to said second experiencing step {*i.e., L2 cache controls update and invalidation of L1 cache*} [col. 10, line 45 - col. 11, line 19].

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch et al. (US6,061,766) and Hazawa (US4,891,809).

As per claim 5, Lynch discloses the claimed invention as detailed above in the previous paragraphs. However, Lynch does not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col.3, lines 38-48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Lynch and Hazawa before him at the time the invention was made, to modify the system of Lynch to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it would have provided a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught y Hazawa.

9. Claims 7-8, 12-13 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,397,300) and Lynch et al. (US6,061,766).

As per claims 7, 12 and 17, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership.

Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership {*i.e., only requests for exclusive use which match cache tags are invalidated*} [Fig. 4; col. 4, lines 19-30].

As per claims 8, 13 and 18, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach third logic which invalidates said corresponding cache memory location in response to a SNOOP hit.

Lynch discloses third logic which invalidates said corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Lynch before him at the time the invention was made, to modify the system of Arimilli to include a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership, logic which invalidates said corresponding cache memory location in response to a SNOOP hit, because it would have provided a snoop process for ensuring cache coherency and an increase in the hit rate of the system as taught by Lynch by invalidating a data object a data object

contained in the on-chip cache and checking for the presence of the data object in the on-chip cache [col. 2, lines 20-21, 34, 60-65] as taught by Lynch.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch et al. (US6,061,766) and Mounes-Toussi et al. (US6,425,060).

As per claim 4, Lynch discloses the claimed invention as detailed above in the previous paragraphs. However, Lynch does not specifically teach fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read.

Mounes-Toussi fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read [col. 8, lines 44-61].

It would have been obvious to one of ordinary skill in the art, having the teachings of Lynch and Mounes-Toussi before him at the time the invention was made, to modify the system of Lynch to include fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read because it would have provided a data processing system which maintains coherence by using a multi-level coherence mechanism that relies on appropriate requests and replies transferred between the various memories in a shared memory system [col. 8, lines 36-41] as taught by Mounes-Toussi.

11. Claim 9, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,397,300) and Mounes-Toussi et al. (US6,425,060).

As per claims 9, 14 and 19, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss.

Mounes-Toussi discloses fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss [col. 8, lines 44-61].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Mounes-Toussi before him at the time the invention was made, to modify the system of Arimilli to include fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read because it would have provided a data processing system which maintains coherence by using a multi-level coherence mechanism that relies on appropriate requests and replies transferred between the various memories in a shared memory system [col. 8, lines 36-41] as taught by Mounes-Toussi.

12. Claims 10, 15 and 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,397,300) and Hazawa (US4,891,809).

As per claims 10, 15 and 20, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col. 3, lines 38-48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Hazawa before him at the time the invention was made, to modify the system of Arimilli to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it would have provided a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught y Hazawa.

***Response to Arguments***

13. Applicant's arguments filed June 12, 2003 have been fully considered but they are not persuasive. As to the remarks, applicant asserted that:

(a) Lynch has no "level three cache memory" and does not show a "system bus".

Examiner respectfully traverses applicant's arguments for the following reasons. Applicant's assertion that examiner admits that Lynch does not teach a "third level cache" and a "system bus" is clearly erroneous. As previously mentioned on page 9 of the Final Office Action mailed April 9, 2003 (Paper No. 5), Examiner would like to emphasize that Lynch does disclose a "level three cache memory". Contrary to applicant's arguments on page 3 that the examiner wishes to suggest that his rejection is based upon "inherency", Examiner would like to emphasize that it is well known in the art to use "a main memory" as "a level three cache memory". Therefore, the "main memory" equals or constitutes the "level three cache memory". Thus, the rejection is not based upon "inherency". Therefore, there is no burden of proof of inherency to be met as asserted by applicant.

Even though Lynch does not show a system bus in his drawings, Lynch clearly discloses the use of a "system bus" in his disclosure. The "system bus" is represented by a "common memory bus" as previously mentioned on page 9 of the Final Office Action mailed April 9, 2003 (Paper No. 5).

(b) Lynch does not snoop the common memory bus;

Examiner would like to point out that the SNOOP and SHARE signals of Lynch are in communication with the external components and the SIU 312 as shown in Fig. 3. Note that when a SNOOP arrives to the SIU 312, a response is returned from the e-cache (col. 3, line 66- col. 4, line 3). Further note that access to and from the main memory of Lynch can only occur through the e-cache 306 via the common memory bus as detailed in column 3, lines 34-38. Thus, the "common memory bus", being an external component, must be SNOOPed for address matching and handshake purposes.

(c) Examiner has impermissibly read the claimed "second logic" and "third logic" structures on to a single structure of Lynch.

The use of "second and third logics" constitutes an inherent feature of the Lynch reference of record. Considering that logic steps are used as aids in showing the way a proposed program will work and that each step processes information by performing a logical operation on it, it is clearly obvious that any computer system uses a combination of logics to produce outputs based on the rules of logic it is designed to follow. Thus, multiple logics must be used as part of the system to obtain desired results.

(d) The examiner does not specify which reference or where within that reference the motivation for the rejection of claim 5 is extracted.

Examiner would like to point out that the reference along with the portion used to extract the motivation was previously cited on page 6 of the Office Action mailed April 9, 2003. For applicant's convenience, Examiner would like to reiterate that the motivation and likelihood of success were extracted from the Hazawa reference of record in column 1, lines 30-37.

(e) Arimilli has no "level three cache memory" and does not show a "system bus".

Examiner respectfully traverses applicant's arguments for the following reasons. Applicant's assertion that examiner admits that Arimilli does not teach a "third level cache" and a "system bus" is clearly erroneous. It is well known in the art to use "a main memory" as "a level three cache memory". Therefore, the "main memory" equals or constitutes the "level three cache memory".

Arimilli discloses the use of a system bus 105 as detailed in Fig. 4 and column 6, line 50.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach retrieving and recording data in response to L1 and L2 cache misses.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Pierre M. Vital
June 25, 2003